Low-voltage organic field-effect transistors based on novel high-κ organometallic lanthanide complex for gate insulating materials

Qi Liu,[1] Yi Li,[1] Yang Zhang,[1] Huabin Sun,[2] You Song,[1,a] Yun Li,[2,a] Yi Shi,[2] Xizhang Wang,[1,a] and Zheng Hu[1]

[1]*Key Laboratory of Mesoscopic Chemistry of MOE, Jiangsu Provincial Lab for Nanotechnology, School of Chemistry and Chemical Engineering, Nanjing University, Nanjing 210093, China. High-Tech Research Institute of Nanjing University (Suzhou), Suzhou 215123, China*

[2]*School of Electronic Science and Engineering and Jiangsu Provincial Key Laboratory of Photonic and Electronic Materials, Nanjing University, Nanjing 210093, China*

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A novel high-κ organometallic lanthanide complex, $Eu(tta)_3L$ (tta=2-thenoyltrifluoroacetonate, L = 4,5-pinene bipyridine), is used as gate insulating material to fabricate low-voltage pentacene field-effect transistors (FETs). The optimized gate insulator exhibits the excellent properties such as low leakage current density, low surface roughness, and high dielectric constant. When operated under a low voltage of −5 V, the pentacene FET devices show the attractive electrical performance, e.g. carrier mobility (μ_{FET}) of 0.17 $cm^2\ V^{-1}\ s^{-1}$, threshold voltage (V_{th}) of −0.9 V, on/off current ratio of 5×10^3, and subthreshold slope (*SS*) of 1.0 V dec^{-1}, which is much better than that of devices obtained on conventional 300 nm SiO_2 substrate (0.13 $cm^2\ V^{-1}\ s^{-1}$, −7.3 V and 3.1 V dec^{-1} for μ_{FET}, V_{th} and *SS* value when operated at −30 V). These results indicate that this kind of high-κ organometallic lanthanide complex becomes a promising candidate as gate insulator for low-voltage organic FETs. [http://dx.doi.org/10.1063/1.4894450]

I. INTRODUCTION

Organic field-effect transistors (OFETs) have attracted much attention owing to their important applications in large-area, low-cost, and/or flexible electronics.[1–3] Great efforts have been devoted to improving the performance of OFETs.[4] For OFETs, lowering the operating voltages is pursuit of the goal because, to date, the operating voltages still are relatively high, which may lead to high power consumption in organic circuits.[5] The operating voltages can be effectively reduced by increasing the dielectric capacitance per unit area of the gate insulator by decreasing the thickness of insulator or/and using the high dielectric constant (κ) dielectric.[6] The former has been accessed by utilizing self-assembled mono- and multi-layer and polymer thin film as insulators.[7–9] The common high-κ dielectric is inorganic metal-oxides in general.[10–16] Up to now, it still is of great importance to develop novel high-κ materials as gate insulator, especially organic high-κ dielectric. Recently, it is reported that organometallic lanthanide complexes, a kind of neutral mononuclear molecule-based materials, have the merit of good thermal stability, high dielectric constants (high-κ), easy thin film formation by thermal evaporation method.[17] They are thus regarded as promising candidates as gate dielectric materials, especially for the low operating voltage OFETs and/or flexible electronics. Herein, we

[a]To whom correspondence should be addressed. E-mail: wangxzh@nju.edu.cn (X. Z. Wang), yli@nju.edu.cn (Y. Li), yousong@nju.edu.cn (Y. Song).

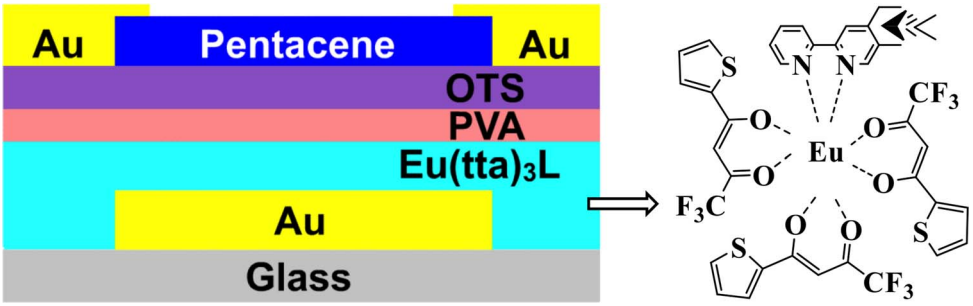

FIG. 1. Schematic diagram of a bottom-gate top-contact OFETs using pentacene as the channel material and a triple-laminated configuration of $Eu(tta)_3L$/PVA/OTS as gate insulator, along with the molecular structure of $Eu(tta)_3L$ (tta = 2-thenoyltrifluoroacetonate, L = 4,5-pinene bipyridine).

report a novel high-κ lanthanide complex, $Eu(tta)_3L$ (tta=2-thenoyltrifluoroacetonate, L=4,5-pinene bipyridine), as gate insulating material to fabricate the low operating voltage pentacene field-effect transistors (OFETs). The triple-laminated gate insulator exhibits excellent properties, including low leakage current density ($\sim 10^{-7}$ A cm^{-2}), low surface roughness (RMS of ca. 0.28 nm), and high dielectric constant of 11. The pentacene OFETs can well work under a low voltage of −5 V and exhibit good electrical performance, e.g. the field-effect mobility (μ_{FET}) of 0.17 cm^2 V^{-1} s^{-1}, threshold voltage (V_{th}) of −0.9 V, and subthreshold slope (*SS*) of 1.0 V dec^{-1}, the μ_{FET}, V_{th}, and *SS* correspond to 0.13 cm^2 V^{-1} s^{-1}, −7.3 V, and 3.1 V dec^{-1} to the analogue common SiO_2 as gate insulator operated at −30 V. Therefore, this kind of lanthanide complex is a good candidate for low-voltage OFETs.

II. EXPERIMENTAL

$Eu(tta)_3L$ was synthesized by the method as described in our recent work, which is insoluble in water.[17] Polyvinyl alcohol (PVA) with the hydrolysis level of about 80% and weight-average molar mass (M_w) of ca. 10000 is used as water-soluble modifier to greatly reduce the effect of organic solvent to the $Eu(tta)_3L$ thin film. The purities of octadecyltrichlorosilane (OTS) and pentacene are 95% and 99%, respectively. All raw materials were purchased from Aldrich and directly used without further purification. Fig. 1 illustrates the schematic diagram of the bottom-gate top-contact architecture of pentacene OFETs and the molecular structure of $Eu(tta)_3L$ as well. In a typical fabrication procedure of pentacene OFETs, the cleaned glass substrate was placed in the chamber and evacuated up to 5×10^{-5} Pa. Au strip with the thickness of 50 nm and the width of 500 μm as gate electrode was firstly deposited onto the glass substrate by thermal evaporation at ca. 10^{-4} Pa. And then, 100 nm thickness of $Eu(tta)_3L$ thin film as gate insulating material was deposited on the Au strip by thermal evaporation at about 150 °C and 10^{-4} Pa. Subsequently, PVA dissolved in deionized water (4 mg ml^{-1}) was spin-coated onto the $Eu(tta)_3L$ film. After annealed at 50 °C for 2 h, OTS monolayer was modified to the surface of PVA layer by vacuum vapor diffusion method. Namely, the as-prepared gate insulator has a triple-laminated structure, which is denoted as $Eu(tta)_3L$/PVA/OTS. Then, 50 nm thickness of pentacene thin film was deposited on the gate insulator by thermal evaporation at 50 °C and ca. 10^{-4} Pa at the deposition rate of 0.1 Å s^{-1}. Finally, Au electrodes were thermally deposited through a shadow mask. Therefore, the OFETs had a bottom-gate top-contact architecture with the channel length (*L*) and width (*W*) of 100 and 500 μm, respectively. As contrast, the OFETs with only $Eu(tta)_3L$ and $Eu(tta)_3L$/PVA thin film as gate insulator were also fabricated. For characterizations of leakage current and capacitance (dielectric constant), a metal-insulator-metal (MIM) structure device was fabricated by direct deposition of 50 nm thickness of Au square with the side length 150 μm onto the $Eu(tta)_3L$/PVA/OTS insulator. The surface morphology and crystal structure of thin films were characterized by atomic force microscopy (AFM, Benyuan Nano-Instruments Ldt., CSPM5500) and X-ray diffraction (XRD, Bruker D8 Advance A25, $K_{\alpha 1}$ = 1.78897 Å, Fe filter of

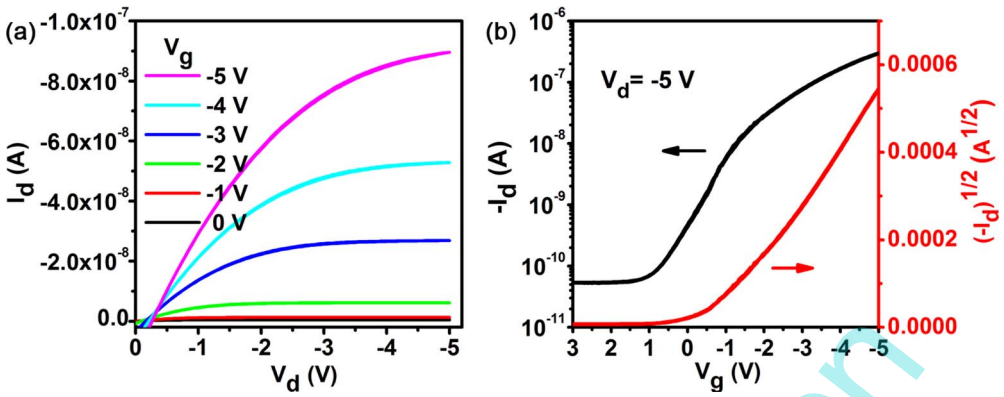

FIG. 2. Output and transfer curves of pentacene OFET using the high-κ triple-laminated Eu(tta)$_3$L/PVA/OTS as gate insulator.

0.02 mm thickness). The capacitance and electronic measurement were carried out using a Keithley 4200-SCS semiconductor parameter analyzer under ambient atmosphere.

III. RESULTS AND DISCUSSION

Fig. 2 shows the typical output and transfer characteristics of pentacene OFET using the triple-laminated thin film of Eu(tta)$_3$L/PVA/OTS as the gate insulator. The pentacene OFET exhibits typical p-type field effect behavior, operated under a negative gate voltage (V_g) and source-drain voltage (V_d), with distinct linear and saturation regions in the output curves shown in Fig. 2(a).[18] Noticeably, the device can effectively work at an operation voltage as low as −5 V. From the transfer curve in Fig. 2(b), field-effect mobility (μ_{FET}), threshold voltage (V_{th}), on/off ratio, and subthreshold slope (SS) are extracted to 0.17 cm^2 V^{-1} s^{-1}, −0.9 V, 5 × 10^3, and 1.0 V dec^{-1}, respectively, which are comparable with and even obvious superior to those of a contrast OFET with a 300 nm SiO_2 as the gate insulator and operated as high as voltage of −30 V (Fig. S1).[19] In addition, the off current is as low as −5 × 10^{-11} A, which means the low leakage current. Moreover, the V_{th} and SS are the indicators for estimating the charge trap density at the interface between a semiconductor and an insulator. The difference in V_{th} (ΔV_{th}) at the semiconductor/dielectric interface is correlated with trapped charge on one side of a capacitor:

$$N_{trap} \approx \frac{C_i \times \Delta V_{th}}{q} \tag{1}$$

the maximum trap density can be calculated by using the value of the SS:

$$N_{trap}^{max} \approx \left[\frac{q\ SS\ \log(e)}{kT} - 1\right]\frac{C_i}{q} \tag{2}$$

where q is the electronic charge, k is Boltzmann constant, and T is the temperature (300 K) and C_i is the gate dielectric capacitance per unit area.[20,21] For Eu(tta)$_3$L/PVA/OTS-based pentacene OFETs, the estimated maximum trap density (N_{trap}) is ca. 1.2 × 10^{12} cm^{-2}. As contrast, the electrical performances of the pentacene OFETs based on Eu(tta)$_3$L and Eu(tta)$_3$L/PVA as gate insulator have also been characterized and shown in Fig. S2.[19] It is clearly seen that their electrical performances are distinctly inferior to those of pentacene OFETs based on the Eu(tta)$_3$L/PVA/OTS as gate insulator, e.g. to Eu(tta)$_3$L insulator, the off current is as high as −6 × 10^{-9} A and on/off current ratio is only 30, which suggests the high leakage current. PVA modification can obviously reduce the leakage current and improve the device performance. Interestingly, the OTS modification can further enhance the electrical performance of pentacene OFETs. Namely, the electrical performance of penetacene OFETs have an order of Eu(tta)$_3$L < Eu(tta)$_3$L/PVA < Eu(tta)$_3$L/PVA/OTS as gate insulator. Such large difference of electrical performance of the devices based on these three gate insulators should strongly depend upon the structure of pentacene thin film, the surface roughness of insulators, the leakage current and dielectric property of insulators.

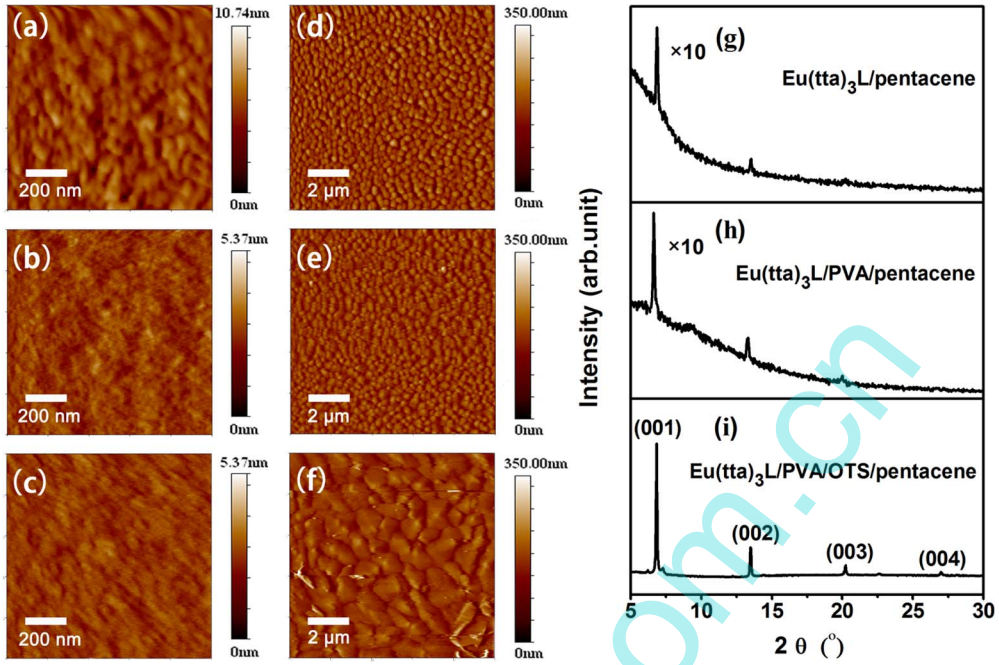

FIG. 3. The surface morphology and crystal structure of gate insulators and pentacene thin films. (a-c) AFM images of $Eu(tta)_3L$, $Eu(tta)_3L$/PVA, and $Eu(tta)_3L$/PVA/OTS as gate insulators. (d-f) AFM images of pentacene thin films deposited on the corresponding insulators of a-c. (g-i) The XRD patterns of pentacene thin films of d-f.

The surface characteristics of thin films are firstly investigated by AFM, including three above-mentioned gate insulators and pentacene thin films deposited on the corresponding insulators. The root-mean-square (RMS) roughnesses of the insulators film are ca. 0.91, 0.33, and 0.28 nm, corresponding to $Eu(tta)_3L$, $Eu(tta)_3L$/PVA, and $Eu(tta)_3L$/PVA/OTS (Fig. 3(a)–3(c)). As known, the small RMS roughness of insulator is beneficial to enhance the device performance. With respect to device fabrication, 0.91 nm RMS roughness of $Eu(tta)_3L$ is too high. Thus, a thin layer of dielectric PVA polymer is spin-coated on $Eu(tta)_3L$ layer to form $Eu(tta)_3L$/PVA bilayer, whose RMS roughness is greatly reduced to the level of 0.33 nm (Fig. 3(b)). To the best of our knowledge, for pentacene OFET, the hydrophobicity of insulator surface favors the improvement of the device performance while the hydrophilicity of insulator surface is a disadvantage factor.[22] Because PAV has a large amount of the hydrophilic hydroxyl groups to increase trap density in the interface of PVA and pentacene layers against the electrical performance, the OTS modification, deposited a self-assembled monolayer, is necessary to transfer the hydrophilic hydroxyl groups to the hydrophobic surface for the electrical performance.[23] To $Eu(tta)_3L$, $Eu(tta)_3L$/PVA, and $Eu(tta)_3L$/PVA/OTS insulators, the morphologies of pentacene grains change from dot-like shape to the common ridge-like shape and the corresponding grain sizes of pentacene obviously increase from ca. 370 and 440 nm to 2,360 nm (Fig. 3(d)–3(f)). Following XRD characterizations of Fig. 3(g)–3(i), the crystallinity of pentacene films also become better and better. AFM and XRD results indicate that the small RMS roughness and hydrophobicity of insulators are in favor of the grain size and crystallinity of pentacene. In general, the low surface roughness of insulator and the large crystallinity of pentacene film benefit the charge transport and electrical performances of pentacene OFETs.[11] Thus, the device performances should become better and better in the order of $Eu(tta)_3L$, $Eu(tta)_3L$/PVA, and $Eu(tta)_3L$/PVA/OTS as insulators, which is supported by the results in Fig. 2 and Fig. S2.[19]

To further investigate the leakage current and dielectric properties of the gate insulators, we intentionally fabricated the device with an MIM structure. Fig. 4(a) shows the typical plot of leakage current density versus bias voltage with $Eu(tta)_3L$/PVA/OTS as insulator. The leakage current density is as low as at the level of 10^{-7} A cm^{-2} at ±5 V bias voltage, which suggests the low off current of pentacene OFET and is consistent with the results in Fig. 2. Fig. 4(b) exhibits the frequency

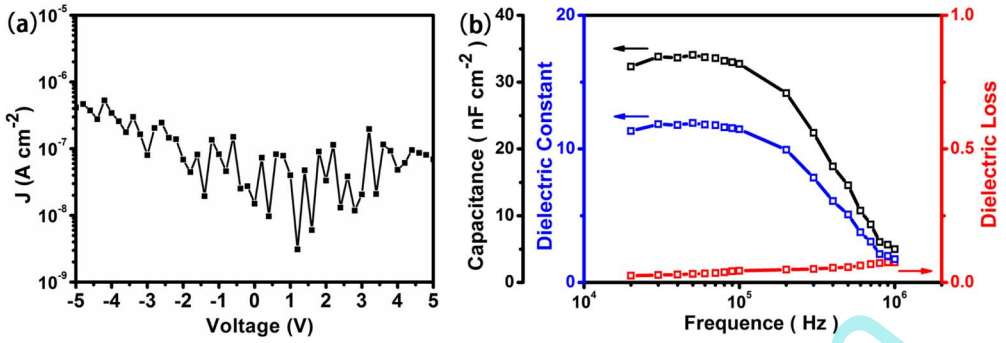

FIG. 4. The electrical characteristics of $Eu(tta)_3L$/PVA/OTS thin film. (a) Plot of leakage current density versus bias voltage of the MIM device. (b) The relationship of dielectric capacitance per unit area, dielectric constant and dielectric loss versus frequency, measured at 0 V bias voltage.

dependence of dielectric capacitance per unit area and dielectric constant for the MIM structure measured under 0 V bias voltage and the frequency in the range of 2×10^4 and 10^6 Hz. The dielectric capacitance per unit area is ca. 33 nF cm^{-2} in the range of 2×10^4 and 10^5 Hz. Because the thickness of the dielectric layer (i.e. gate insulator) is ca. 300 nm, the calculated dielectric constant is 11, far superior to 3.8 of SiO_2. The dielectric loss is lower than 0.1 in the range of the measurement frequency of 2×10^4 and 10^6 Hz. The results indicate that the triple-laminated $Eu(tta)_3L$/PVA/OTS insulator can well meet the requirements of gate dielectric for low-voltage OFETs.

IV. CONCLUSIONS

In summary, we have successfully fabricated low-voltage OFETs by using a high-κ triple-laminated thin film of $Eu(tta)_3L$/PVA/OTS as the gate insulator. The triple-laminated thin film exhibits a relative high-κ value of 11. When operated at −5 V, the corresponding pentacene OFETs show good μ_{FET} of 0.17 cm^2 V^{-1} s^{-1} comparable to that of the analogue OFETs using conventional SiO_2 of 300 nm as insulator operated at −30 V. Interestingly, the V_{th} of −0.9 V and *SS* of 1.0 V dec^{-1} for the device based on $Eu(tta)_3L$/PVA/OTS thin film are significantly superior to V_{th} of −7.3 V and *SS* of 3.1 V dec^{-1} for the one based on conventional SiO_2. Thus, the high-κ metal-organic lanthanide complexes should be a potential candidate for low-voltage OFETs.

ACKNOWLEDGMENTS

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